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E-mail: xytang@mail.xidian.edu.cn Projcet supported by the National Natural Science Foundation of China (Grant Nos. 61404098, 61176070, and 61274079), the Doctoral Fund of Ministry of Education of China (Grant Nos. 20110203110010 and 20130203120017), the National Key Basic Research Program of China (Grant No. 2015CB759600), and the Key Specific Projects of Ministry of Education of China (Grant No. 625010101). Abstract In this paper, the normally-off N-channel lateral 4HSiC metaloxidesemiconductor field-effect transistors (MOSFFETs) have been fabricated and characterized. A sandwich- (nitridationoxidationnitridation) type process was used to grow the gate dielectric film to obtain high channel mobility. The interface properties of 4HSiC/SiO2 were examined by the measurement of HF IV, GV, and CV over a range of frequencies. The ideal CV curve with little hysteresis and the frequency dispersion were observed. As a result, the interface state density near the conduction band edge of 4HSiC was reduced to 2 1011eV1cm2, the breakdown field of the grown oxides was about 9.8MV/cm, the median peak field-effect mobility is about 32.5cm2V1s1, and the maximum peak field-effect mobility of 38cm2V1s1 was achieved in fabricated lateral 4HSiC MOSFFETs. 1. IntroductionDue to excellent physical and electrical properties, such as high breakdown electric field, wide bandgap, high thermal conductivity, and high electron saturation velocity, silicon carbide (SiC) has attracted increasing attention in high-temperature, high-power, and high-voltage devices.[14] Metaloxidesemiconductor field-effect transistors (MOSFETs) based on SiC have been regarded as a promising candidate for low-loss and fast power devices in advanced electronic systems.[5] Significant progress in 4HSiC MOSFETs has been demonstrated recently, with the fabrication of accumulation-mode MOSFETs (ACCUFETs),[1] UMOSFET,[2,6] DMOSFET,[710] and RESURF MOSFET.[11] SiC lateral MOSFETs are also very attractive as high-frequency power transistors, which can favorably compete with Si lateral MOSFET.[11,12] SiC lateral devices have a distinctive advantage of being able to be integrated with other devices, reducing cost, and enhancing overall circuit performance.[11,13]The growth of high-quality gate oxides (SiO2) with abrupt SiC/SiO2 interfaces, containing a low density of interface traps Dit, is crucial for the fabrication of reliable MOSFETs with high channel mobility on 4HSiC.[14] The main source of the high Dit values has been attributed to residual carbon in the gate oxide layer,[15] which was observed in the form of clusters[16,17] distributed along the SiO2/SiC interface. Although the chemical nature of these clusters is still not completely understood, it has been related to carbon complexes and silicon oxycarbides (SiCxOy)[18] formed during the oxidation process. To form high-quality gate oxides with abrupt SiC/SiO2 interfaces, here a sandwich gate oxidation method[14] was used in our work. In this paper, our recent experimental work on N-channel enhancement lateral 4HSiC MOSFFETs is reported. The lateral 4HSiC MOSFFETs were successfully fabricated using ion implantation and sandwich (nitridationoxidationnitridation) type gate oxidation process. N-type MOS capacitors were also fabricated simultaneously with the lateral devices to investigate the interface properties of 4HSiC/SiO2. The properties of 4HSiC/SiO2 interfaces on N-type MOS capacitors were examined by the measurement of HF CV, IV, and GV over a range of frequencies. High mobility of 38cm2V1s1 was achieved for the fabricated lateral 4HSiC MOSFFETs.2. ExperimentsN-type 4-off 4HSiC (0001) Si-face epilayer with a net donor concentration of 6 1015cm3 was used to fabricate N-type MOS capacitors and lateral N-channel 4HSiC MOSFFETs. A schematic cross section of the lateral N-channel 4HSiC MOSFFETs and scanning electron microscopy (SEM) image of the fabricated device cross section are shown in Fig.1. Figure2 shows a top view photograph of a fabricated device with channel length of 10m and channel width of 200m. The P-well was formed by multiple-energy Al+ implantation of a box profile at three energies (40350keV). The N+ source and drain regions were created by nitrogen implantation of a box profile. The P+-region was also formed by high-dose Al+ implantation for obtaining good ohmic contacts on the p-well. After implantation, activation annealing was carried out in Ar at 1650C for 30min. All wafers were protected with a carbon cap to minimize the surface roughness during annealing, and hereafter, the carbon cap was removed by low temperature thermal oxidation.Fig.1.Figure OptionFig.1. (a) Schematic cross section of the fabricated lateral N-channel 4HSiC MOSFFETs and (b) scanning electron microscopy (SEM) image (cross section) of fabricated device.Prior to gate oxidation, the samples were prepared using RCA cleaning. The gate oxides were formed by the an NO/O2/NO sandwich-type process, which consists of a 2% NO pre-anneal for 1 hour, followed by the bulk oxide growth in 5% dry O2, finalized with a post oxidation anneal in 2% NO for an hour.[2] Next, a polysilicon film was deposited and patterned to form the gate contact. Finally, source and drain Ohmic contacts were formed by evaporating Ti/Ni/Al (50nm/100nm/200nm) and annealing with rapid thermal processing (RTP).Thicknesses of the gate dielectric films were determined by both scanning electron microscopy (SEM), and capacitancevoltage (CV) measurements. The channel length (Lch) and width (Wch) of the fabricated lateral MOSFETs were 10m and 200m, respectively. The MOS capacitors and MOSFET electrical properties (transfer and output characteristics) were measured with the Agilent B1505A semiconductor characterization system. All measurements presented in this paper were performed at room temperature.3. Results and discussionFigure3 shows the bidirectional capacitancevoltage (CV) characteristics measured with various frequencies from 10kHz to 1MHz for the MOS capacitor fabricated with NO/O2/NO sandwich oxidation. It can be seen that there is almost no hysteresis and frequency dispersion in the CV curves. A relatively small hysteresis (about 0.025 V), corresponding to less border traps Nit near the interface (shown in Table1), is observed in CV curves. This is also confirmed by the conductance values, plotted in Fig.4. For comparisons, the ideal CV curve calculated using Poissons equation was also inserted in Fig.3. It can be seen that the shape of the measured CV curves is very similar to the theoretically calculated CV curve (black dashed line), but there is a small voltage deviation between them, which indicates that there is relatively good quality of 4HSiC/SiO2 interface.Fig.3.Figure OptionFig.3. Bidirectional capacitancevoltage (CV) characteristics measured with various frequencies from 10kHz to 1MHz for the MOS capacitor fabricated with NO/O2/NO sandwich oxidation.Fig.4.Figure OptionFig.4. Conductancevoltage (GV) and capacitancevoltage (CV) curves at 10kHz for the MOS capacitor fabricated with NO/O2/NO sandwich oxidation.Table 1.Table 1. Table 1. Parameters of the MOS capacitor extracted from the CV curve measured at 10kHz.. Parameters Value Nit/cm2 1.93 108 VFB/V 0.71 Neff/cm2 1.39 1011 t/nm 58 Dit @0.2eV/cm2eV1 2 1011 Table 1. Parameters of the MOS capacitor extracted from the CV curve measured at 10kHz..Table1 lists the dielectric thickness (t), flat-band voltage shift (VFB), effective dielectric charge (Neff) extracted from CV measurements. Parameter t was calculated from the maximum accumulation capacitance (Cox). The Neff was obtained from (VFBCox)/qA, where VFB is the VFB shift from the ideal value, A is the area of the capacitor, and q is the electronic charge. Figure5 shows the distribution of interface state density (Dit) near the conduction band edge (Ec) of 4HSiC estimated using the hi-lo CV method. As shown in Fig.5, the trap density (Dit) at 0.2eV below the conduction band edge is as low as 2 1011cm2eV1, which indicates that NO/O2/NO sandwich-type process can reduce the interface state density significantly.Fig.5.To evaluate the dielectric film breakdown characteristics, the typical currentelectric field curves (IE) of fabricated N-type 4HSiC MOS structures is shown in Fig.6, which is transformed from IV curves. The electric field is approximated by (VgVFB)/t, where Vg and t are the gate voltage and the oxide thickness. From Fig.6, it shows that the critical breakdown electric field of SiO2 is about 9.8MV/cm at leakage current only 50nA, and the statistical value of 20 measured MOS structures show that the median breakdown electric field is about 9MV/cm.Figure7 shows the typical output characteristics of the fabricated lateral enhancement mode N-channel MOSFET with the gate voltage (Vg) from 0V to 24V and the drainsource voltage (VDS) from 0V to 15V. The device exhibits a drain current of 900A at Vg = 24V and VDS = 15V. The output characteristics exhibit excellent linear and saturation region. Figure8(a) shows transfer characteristics at room temperature for the fabricated devices measured at a drain voltage of 100mV. The threshold voltage of 9.5V is obtained by linear extrapolation from the linear region of the transfer characteristics. Figure8(b) shows the transconductance versus the gate voltage Vg, in which a peak value of 3.68S is reached at gate voltage of 14V.Fig.7.Figure OptionFig.7. Typical output characteristics of the lateral enhancement mode N-channel MOSFET with gate voltage (Vg) from 0V to 24V and the drainsource voltage (VDS) from 0V to 15V.Fig.8.Figure OptionFig.8. (a) Transfer characteristics of the fabricated devices measured at a drain voltage of 100mV and (b) the corresponding transconductance characteristics.To examine the validity of the NO/O2/NO sandwich-type gate oxidation method, gate voltage dependence of the field-effect mobility FE was measured, and the Vg for the measurement ranges from 0 to 20V. The FE can be calculated from the following formula using transconductance characteristic at the drain voltage of 100mV: where Lch and Wch are the channel length and width, respectively, ID is the drain current, Ro is the contact resistance, and Cox is the oxide capacitance extracted from MOS capacitors. Figure9 shows the field-effect mobility FE as a function of gate voltage Vg in fabricated lateral MOSFETs. The mobility increases at low values of Vg, reaches a peak at the gate bias slightly higher than the threshold voltage, and then decreases. Maximum peak field-effect mobility of 38cm2V1s1 was achieved. The statistic value of field-effect mobility FE of 18 measured samples indicates that the median peak field-effect mobility is about 32.5cm2V1s1. The results show that the sandwich gate oxidation method is helpful to reduce the interface defects and increase the channel mobility.4. ConclusionThe normally-off N-channel lateral 4HSiC metaloxidesemiconductor field-effect transistors (MOSFFETs) have been fabricated using sandwich (nitridationoxidationnitridation) type process in this paper. The interface state density near the conduction band edge of 4HSiC was reduced to 2 1011eV1cm2, breakdown field of the grown oxides was about 9.8MV/cm, and peak field-effect mobility of 38cm2V1s1 was achieved. It is found that the NO/O2/NO sandwich-type oxidation process has a great potential as an alternative gate oxidation method in SiC MOS-based transistors. 12 December 2018 Hebei Semiconductor Research Institute and Institute of Microelectronics in China claim record power figure of merit performance for polymorph gallium oxide (-Ga2O3) metal-oxide-semiconductor field-effect transistors (MOSFETs) [Yuanjie Lv et al, IEEE Electron Device Letters, 14 November 2018]. The 50MW/cm2 figure of merit represents a high breakdown voltage combined with a low on-resistance. High performance of one or the other factor usually entails a reduced characteristic on the other side of the trade-off. The high figure of merit was achieved by using a source-connected field plate to reduce peak electric fields, increasing breakdown performance. Ion implants in the source and drain regions of the devices reduced contact resistance to 1.0-mm. The wide 4.5-4.9eV bandgap of -Ga2O3 suggests that a high critical electric breakdown field of order 8MV/cm is possible in the material. In theory it should be possible to reach a power figure of merit in the range 34,000MW/cm2, so there is clearly much scope for development and optimization work. Before the Hebei/Institute of Microelectronics work the highest reported power figure of merit was 10MW/cm2. Figure 1: (a) Schematic cross section of source-field-plated -Ga2O3 MOSFET, and scanning electron microscope images of (b) surface and (c) cross section of device. The substrate for metal-organic chemical vapor deposition (MOCVD) was iron-doped semi-insulating (010) -Ga2O3. The precursors were trimethyl-gallium and oxygen delivered at 8Torr pressure. The substrate temperature was 750C. Silicon (Si) doping for the 240nm n-type channel layer (Figure 1) was provided by silane (SiH4) flow. Van der Pauw measurements gave an electron density of 1.95x1013/cm2 with 90cm2/V-s mobility, giving a sheet resistance ~3.6k/square. Inductively coupled plasma (ICP) etch was used to give a 350nm-high mesa for device fabrication. Source and drain regions were created with multiple implantations of silicon ions to a depth of ~210nm. Simulations predicted that the surface silicon concentration would be around 1020/cm3. After annealing the doping implants, Ohmic source/drain (S/D) contacts were formed with the deposition of titanium and gold. The gate (G) stack consisted of 25nm of 250C atomic layer deposition (ALD) aluminium oxide (Al2O3) and nickel/gold metal electrode. The aluminium oxide was annealed before electrode deposition. Surface passivation was provided by 400nm plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN). After reactive-ion etch to expose the source and drain metal, the nickel/gold source-connected field plate that extended 2m toward the drain was formed. The 1.5m-long gate was 40m wide. The gate-source distance was 2m. Devices with gate-drain spacings of 7.5m and 14.5m were fabricated. The respective source-drain distances were 11m and 18m. With the gate at 5V, the saturation drain current was 267mA/mm for the 11m source-drain device and 222mA/mm for the 18m version. Under the same gate potential, the low drain bias on-resistance was 41.6-mm in the 11m source-drain transistor. With 20V drain bias, the maximum transconductance for the 11m MOSFET was 10.5mS/mm. The 0.1mA/mm threshold gate voltage was at 50.5V. Gate leakage was around 7.1x10-7A/mm. The researchers see this value as being comparatively large, adding that the culprit may be Al2O3/Ga2O3 interface traps. They suggest that these traps could be reduced with a better optimized surface-state treatment. Further evidence of interface traps was given by ~0.8V hysteresis in the response under forward and reverse sweeps of gate voltage. The on/off current ratio was of the order 106. Figure 2: Three-terminal off-state breakdown characteristics of -Ga2O3 MOSFET with and without source-field plate for (a) 11m and (b) 18m source-drain distance devices. (c) Plot of Ron,sp versus Vbr for Hebei/Institute of Microelectronics devices (this work) and other reported lateral Ga2O3 MOSFETs. Destructive breakdown performance in air was carried out with the gate at -55V (Figure 2). Without source field plates, the breakdown voltages (Vbr) were 310V and 260V for the 18m and 11m MOSFETs, respectively. These values were greater than the 218V value expected from a one-sided abrupt-junction model. The researchers suggest that the better-than-theory result is due to non-uniformity of channel doping and depletion from interface states. Adding source field plates increased the breakdown to 480V in the 11m device and 680V in the 18m MOSFET. Multiplying the on-resistance by the source-drain distance to give a specific on-resistance (Ron,sp), the researchers found values of 4.58m-cm2 and 11.7m-cm2 for the 11m and 18m devices, respectively. Our fabricated devices in this work show much lower Ron,sp compared with other -Ga2O3 MOSFETs and also with the theoretical performance of Si-based power devices, the team comments. The power figure of merit given by Vbr2/Ron,sp was thus 50.4MW/cm2. Although the saturation drain current is still lower than in reported nanomembrane Ga2O3 devices, the researchers claim that their source-field-plated MOSFET shows a record maximum drain current and power figure of merit among devices fabricated on homoepitaxial -Ga2O3. The researchers suggest that increasing the channel layer thickness in conjunction with gate recessing could lead to lower on-resistance and associated improvement in the power figure of merit. Gallium oxide metal-oxide-semiconductor field-effect transistorsMOSFETs The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997. To ensure we keep this website safe, please can you confirm you are a human by ticking the box below. If you are unable to complete the above request please contact us using the below link, providing a screenshot of your experience. Share copy and redistribute the material in any medium or format for any purpose, even commercially. Adapt remix, transform, and build upon the material for any purpose, even commercially. The licensor cannot revoke these freedoms as long as you follow the license terms. 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